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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/561,625	12/19/2005	Andrei Terechko	NL02 1505 US	8452

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
04/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/561,625	TERECHKO ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-30* is/are allowed.

6)☒ Claim(s) *1,2,8-12,14-17,19,20,25 and 26* is/are rejected.

7)☒ Claim(s) *3-7,13 and 21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 and 19-30 are presented for examination. Claim 18 is canceled.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-2, 8, 9, 11, 12, 14-20, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Launiainen (Launiainen), U.S. patent no. 7,114,089.

As per claim 1, Launiainen discloses a circuit arrangement [fig. 3b], comprising a plurality of hardware resources [M1, M2, D1, D2, L1, L2, S1, S2, col. 5, lines 19-25], wherein each hardware resources has a power mode configurable between at least first and second power consumption states [normal mode, power saving mode, col. 5, lines

30-41; col. 6, lines 40-44]; and a processor [1, fig. 5] coupled the plurality of hardware resources [figures 3a, 5], the processor configured to process program code that includes at least one power control instruction [SWFU 00011000] that includes an operand [00011000 602, fig. 6] having power control information disposed therein, wherein the processor is configured to process the power control instruction by selectively setting power modes of at least two hardware resources [D1, D2] among the plurality of hardware resources [M1, M2, D1, D2, L1, L2, S1, S2, col. 5, lines 19-25] based upon the power control information disposed in the power control instruction [SWFU 00011000], and wherein the processor is further configured to maintain the power modes of the power modes of the at least two hardware resources to that specified in the power control instruction while processing at least one subsequent instruction in the program code [figures 3b, 6; col. 6, lines 11-60; col. 7, line 46- col.8, line 27].

In summary, Launiainen teaches a method for using a power control instruction for selectively setting the power mode of the hardware resources. In the disclosed example, the system has 8 hardware resources [M1, M2, D1, D2, L1, L2, S1, S2, col. 5, lines 19 – 22]. The power control instruction has the format of op code [SFWU] and operand[1] [xxxxxxxx] wherein x is 1 or 0 for the two power states embodiment. The operand has 8 bits with one bit per hardware resource. Based upon the operand, the system can selectively change the power mode of at least two hardware resources [D1, D2, 602, fig. 6].

As per claim 2, Launiainen discloses the power control instruction further includes an opcode that uniquely identifies the power control instruction [fig. 6; col. 6, lines 11-47; col. 8, lines 10-20].

As per claim 8, Launiainen discloses that each hardware resource is selected from the group consisting of a register file, a register bank, a register, a cache, a bus interface unit, a bus, a functional unit, a functional block and an instruction decoder [fig. 3b; col. 5, lines 11-27].

As per claim 9, Launiainen discloses that the processor is configured to process explicitly parallel instructions, and wherein the power control instruction comprise an operation among a plurality of operations in an explicitly parallel instruction [col. 6, lines 11-60; col. 7, lines 47-27].

As per claim 11, Launiainen discloses a superscalar processor [col. 1, lines 59-60].

As per claim 12, Launiainen discloses that the processor is configured to assign a side effect to the power control instruction to limit run-time speculation thereof [col. 6, lines 11-50; col. 7, lines 47-64].

As per claim 14, Launiainen discloses that the pluralities of hardware resources are disposed in the processor [fig. 3b].

As per claim 15, Launiainen discloses that at least one hardware resource is disposed outside of the processor but on the same integrated circuit as the processor [fig. 3a].

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[1] It is noted that the right hand side portion of the instruction is the operand. See fig. 6. For example, MVK

As per claim 16, Launiainen discloses that at least one hardware resource is disposed on a separate integrated circuit from the processor [fig. 5].

As per claim 17, Launiainen discloses an integrated circuit [fig. 3a].

As to claims 19, 20, 25 and 26, claims 1, 2, 8-9 basically are the corresponding elements that are carried out the method of operating steps in claims 19, 20, 25, 26. Accordingly, claims 19, 20, 25 and 26 are rejected for the same reason as set forth in claims 1, 2, 8 and 9.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Launiainen (Launiainen), U.S. patent no. 7,114,089 in view of what was well known in the art, as exemplified by Dinechin (Dinechin), U.S. publication no. 2003/0177482.

As per claim 10, Launiainen fails to disclose that a VLIW processor and an EPIC processor.

Examiner takes Official Notice that a VLIW processor and an EPIC processor are well known in the art, evidence of which may be found in

Dinechin: figure 1; paragraph 0005.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the type of processor to improve the functionality of the system.

Allowable Subject Matter

6. Claims 3-7,13, 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

.S2 6, B0. Clearly 6 and B0 are the operand of the MVK instruction. Similarly, 00011000 [602] or

7. Claims 27-30 are allowed over prior art.

Response to Arguments

8. Applicant's arguments filed on 2/21/2008 have been fully considered but are moot in view of new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11011011 [601] is the operand of SWFU.

/Chun Cao/

Primary Examiner, Art Unit 2115

4/4/08

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	10/561,625	TERECHKO ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	